

Application No. 09/516,800  
Attorney Docket No. 12-1038

**REMARKS**

The present application includes claims 1-30. Claims 1-30 were rejected. By this Amendment, claims 1 and 16 have been amended.

Claims 1-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Burch, U.S. Patent No. 5,680,422, in view of Gaudet, U.S. Patent No. 6,285,726. Burch teaches a method and apparatus for reducing waiting time jitter in pulse stuffing synchronized digital communications. As shown in Figure 6 of Burch and described beginning at Col. 6, Line 50, a phase comparator 137 compares an incoming write clock output on link 54 with a reference clock on link 136. The output of the phase comparison is transmitted on link 138 to a digitally controlled phase adjuster 135.

The base reference clock is originally received from the clock generator 64 and then passed to the nominal data clock generator 133 to condition the frequency to the data clock as described at Col. 7, Lines 1-8. The nominal data clock generator 133 passes the reference clock to the digitally controlled phase adjuster 135 which may adjust the phase of the reference clock before passing the reference clock to the phase comparator 137 for comparison with the received write clock.

That is, Burch teaches the use of a single reference clock. Specifically, the comparison of the received data clock with a single reference clock. Even though the reference clock originally developed by the clock generator 64 may be altered in phase and/or frequency, only a single reference clock is compared with the received data clock at the phase comparator 137.

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Gaudet teaches a 10/100 Mb Clock recovery architecture. In Gaudet, a single clock is provided that may be phase shifted a varying amount using N phase shifters. Gaudet clearly recites comparison with a single reference clock in several places. For example, at Col. 4, Lins 13-17 "A single clock generation module (CGM) and N phase multiplexers, ... is used to select one of M phased of a 250MHz clock signal from the CGM for a clock recovery module (CRM)." This is also described beginning at Col. 6, Line 1.

Thus, Gaudet also only teaches a single reference clock for comparison with received data. Although the architecture of Gaudet may be operated in either 10Mb or 100Mb mode, only one mode is available for comparison at any one time.

Thus neither Burch nor Gaudet teach the use of a plurality of reference clocks to form the phase comparison in order to provide additional fidelity and ambiguity resolution. The use of a plurality of reference clocks is recited in the present application beginning at page 6, line 7 and shown in Figures 1-3.

The present application includes independent claims 1 and 16, both of which have been amended to recite the limitation of a plurality of reference clocks generating a plurality of reference signals and using said plurality of reference clocks to generate a phase estimate. Consequently, the Applicant respectfully submits that claims 1 and 16 and their respective dependent claims 2-15 and 17-30 are free of the prior art and allowable.

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**CONCLUSION**

If the Examiner has any questions or the Applicant can be of any assistance, the Examiner is invited and encouraged to contact the Applicant at the number below.

The Applicant herewith petitions the Commissioner of Patents and Trademarks to extend the time for reply to the Office Action mailed May 6, 2003 for one month from August 6, 2003 to September 6, 2003. Because September 6, 2003 falls on a Saturday, the period for reply is automatically extended to Monday, September 8, 2003. Please charge the Deposit Account below to cover the cost of the extension.

The Commissioner is authorized to charge any necessary fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Date: September 8, 2003

  
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